

FIG. 1

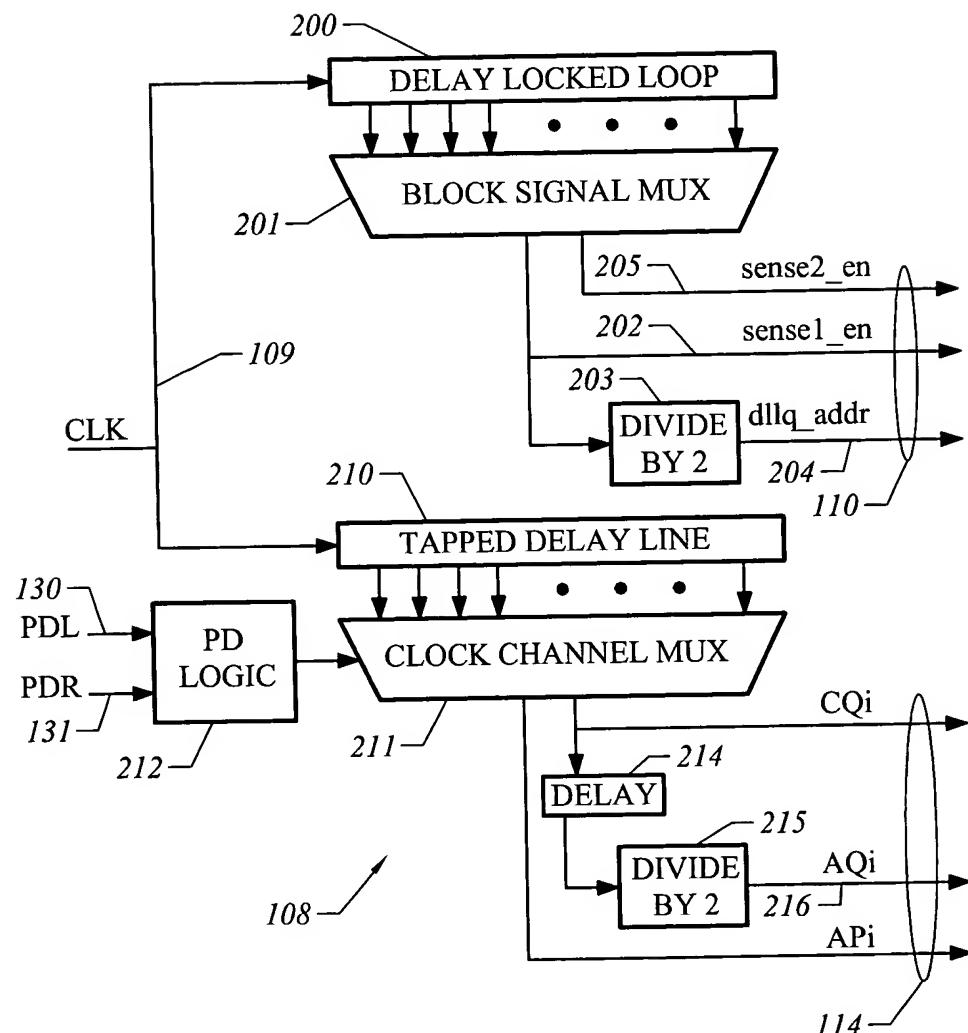


FIG. 2

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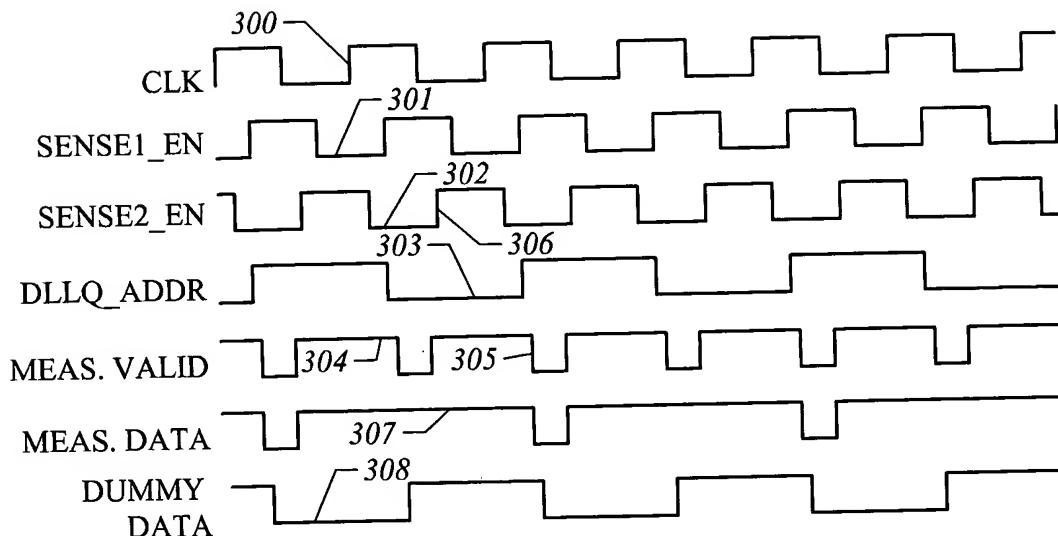


FIG. 3

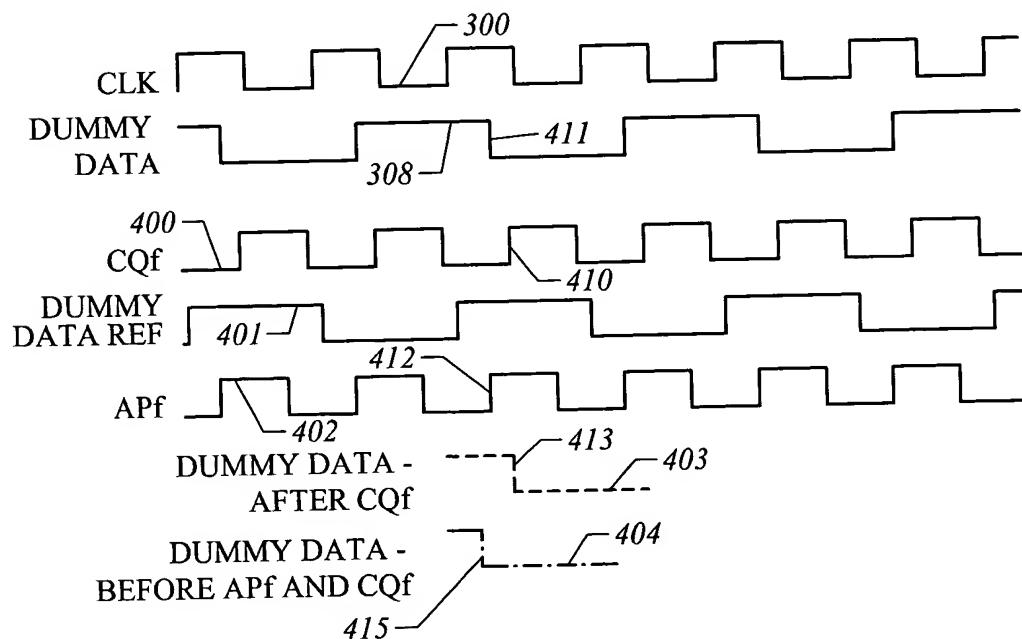


FIG. 4

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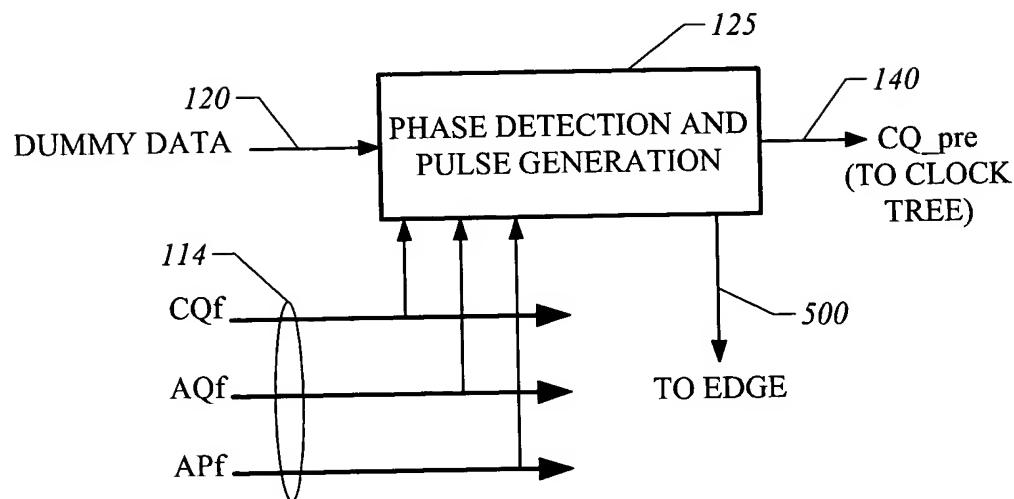


FIG. 5

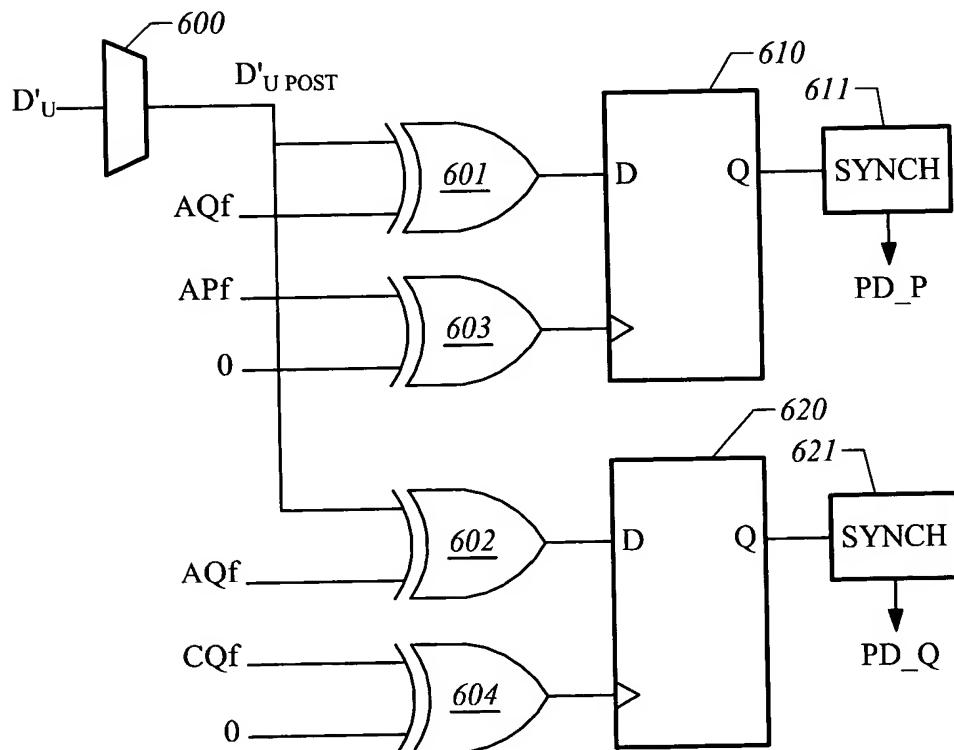


FIG. 6

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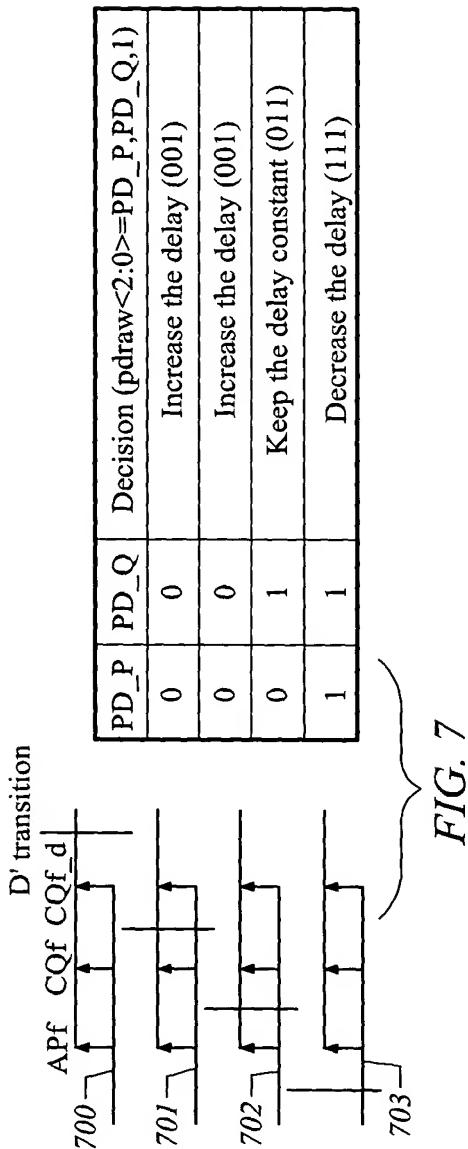


FIG. 8

PDX<0>=NAND(pdraw_u<1>, pdraw_1<1>)
 PDX<1>=AND(pdraw_u<2>, pdraw_1<2>)

PDR<1:0>	PDL<1:0>	Decision
Increase (01)	X	Increase the delay
X	Increase (01)	Increase the delay
Decrease (10)	Decrease (10)	Decrease the delay (Only if the request is repeated for n cycles, n=k* #(scanned banks in one quadrant))
All other cases		Keep the delay constant

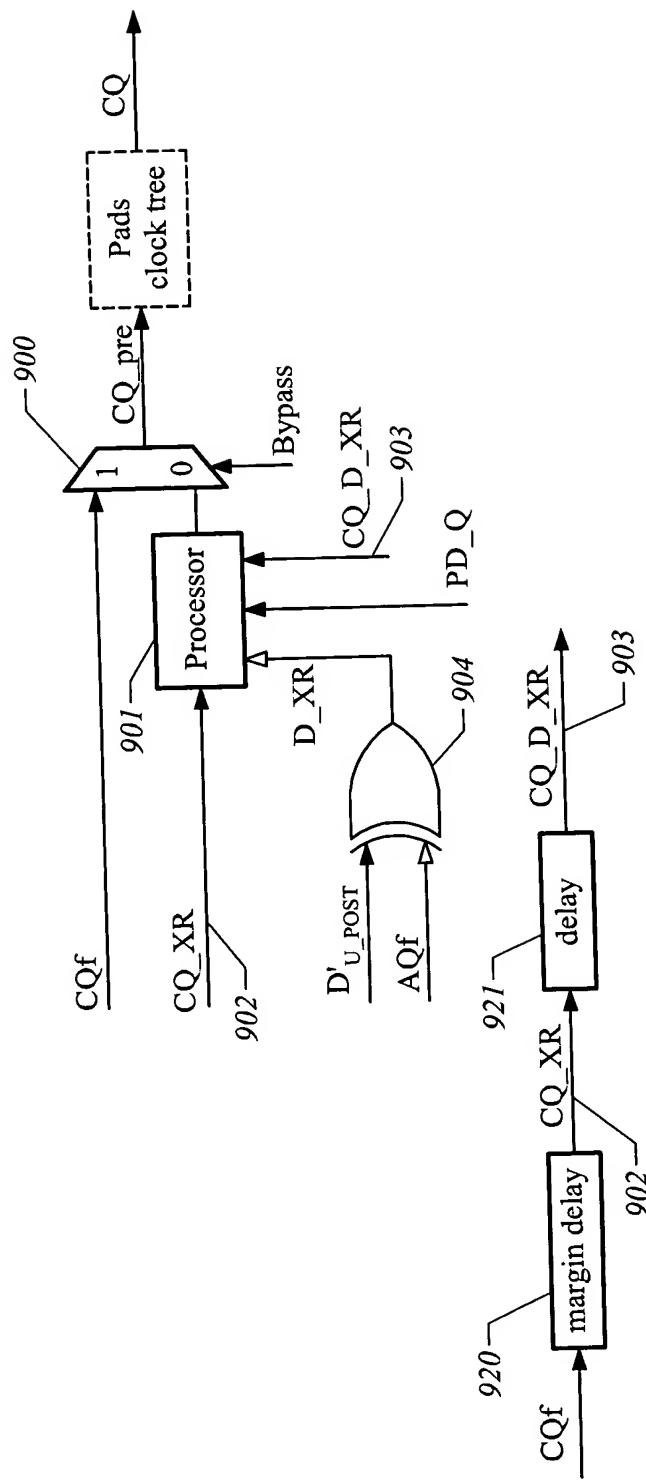


FIG. 9

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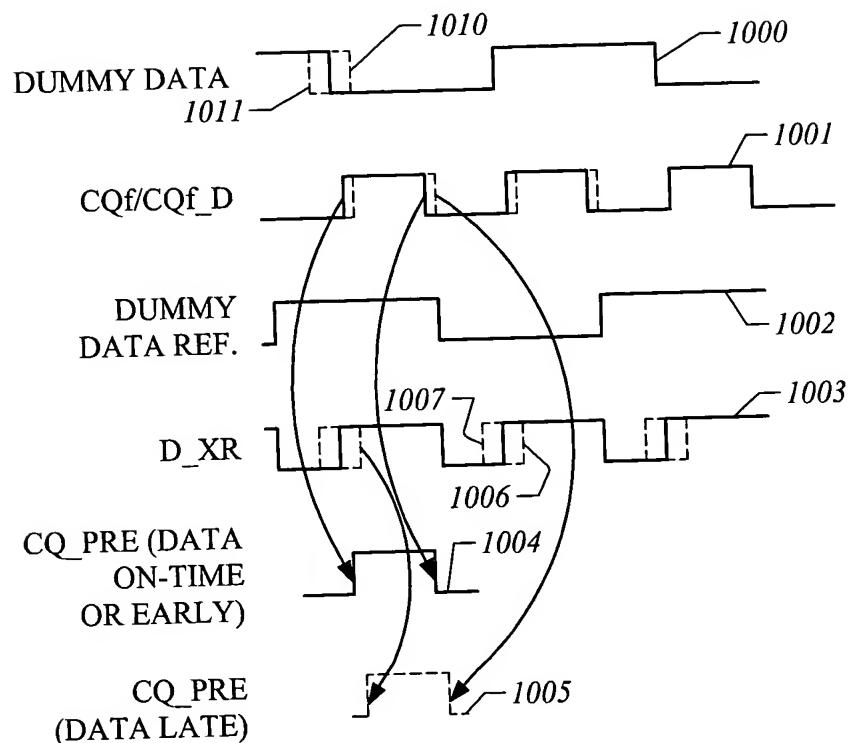


FIG. 10

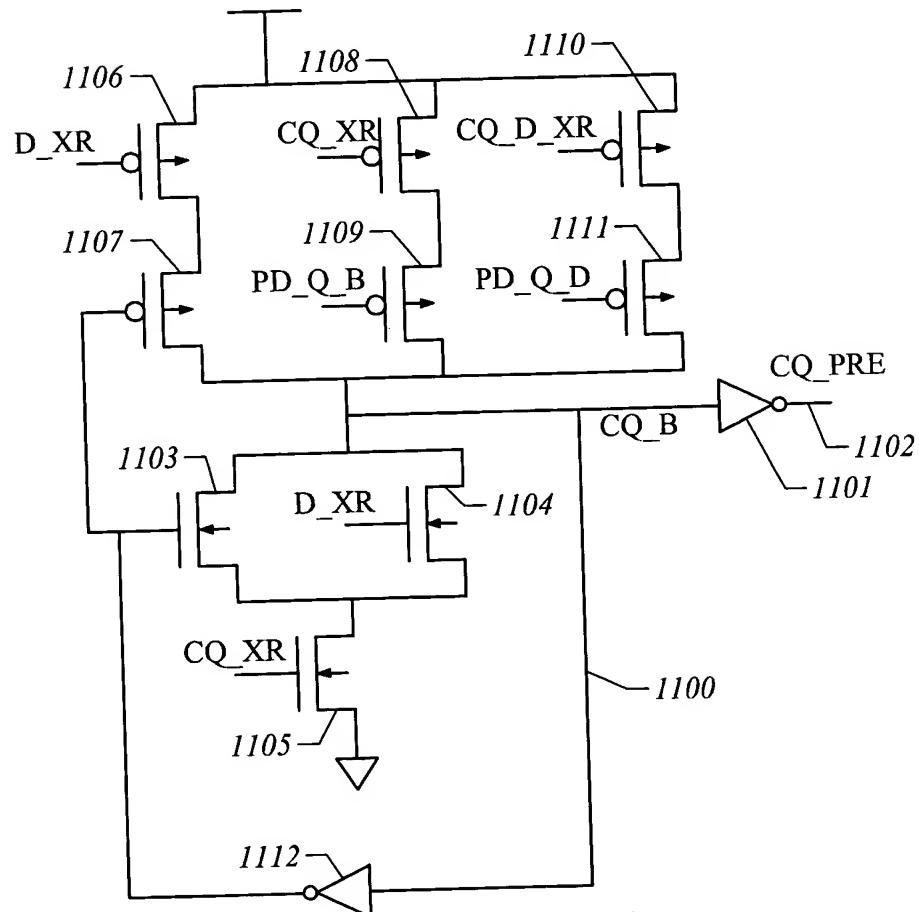


FIG. 11

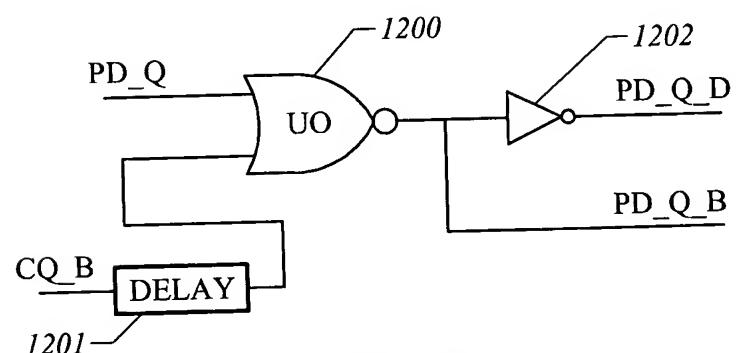


FIG. 12

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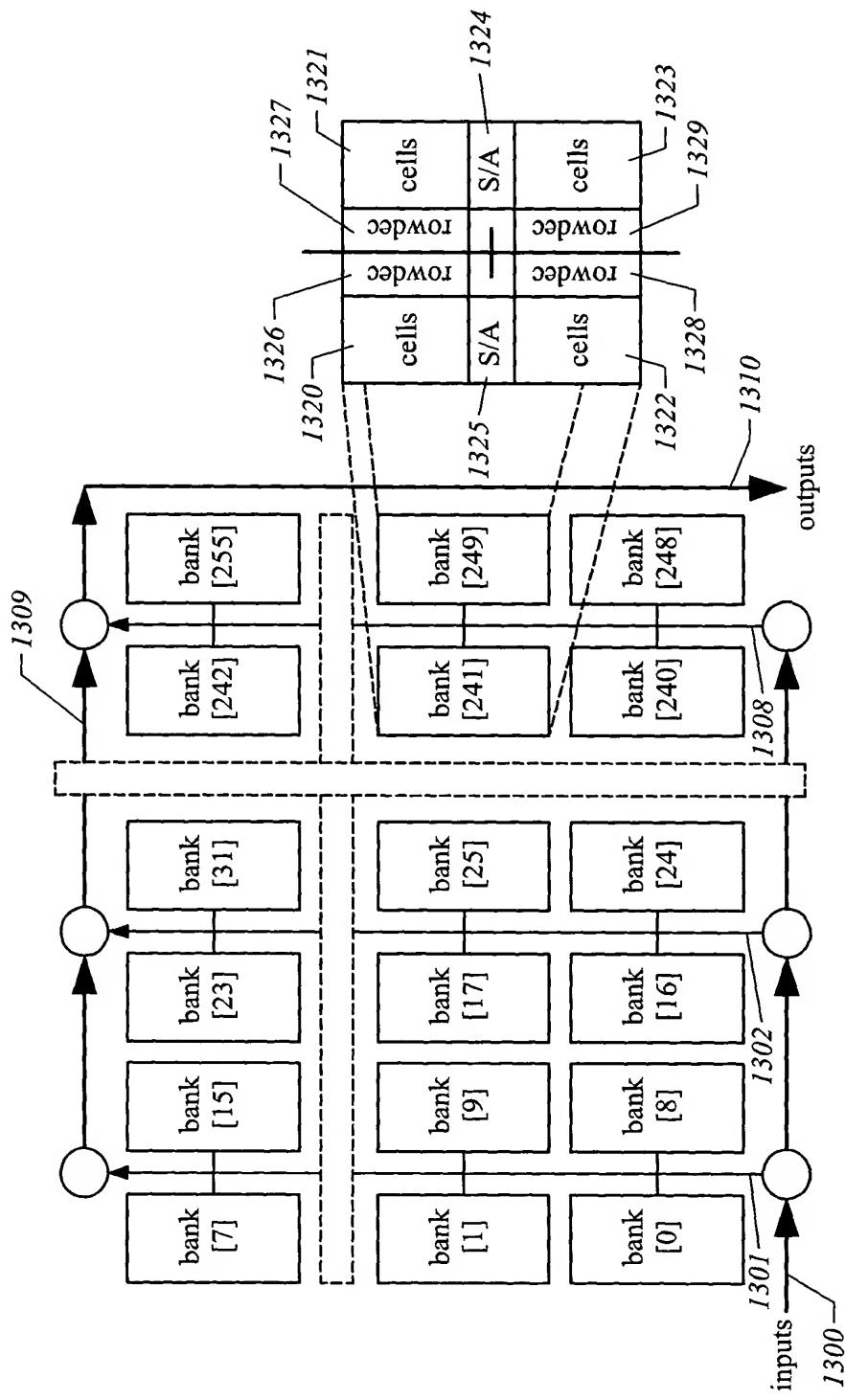


FIG. 13

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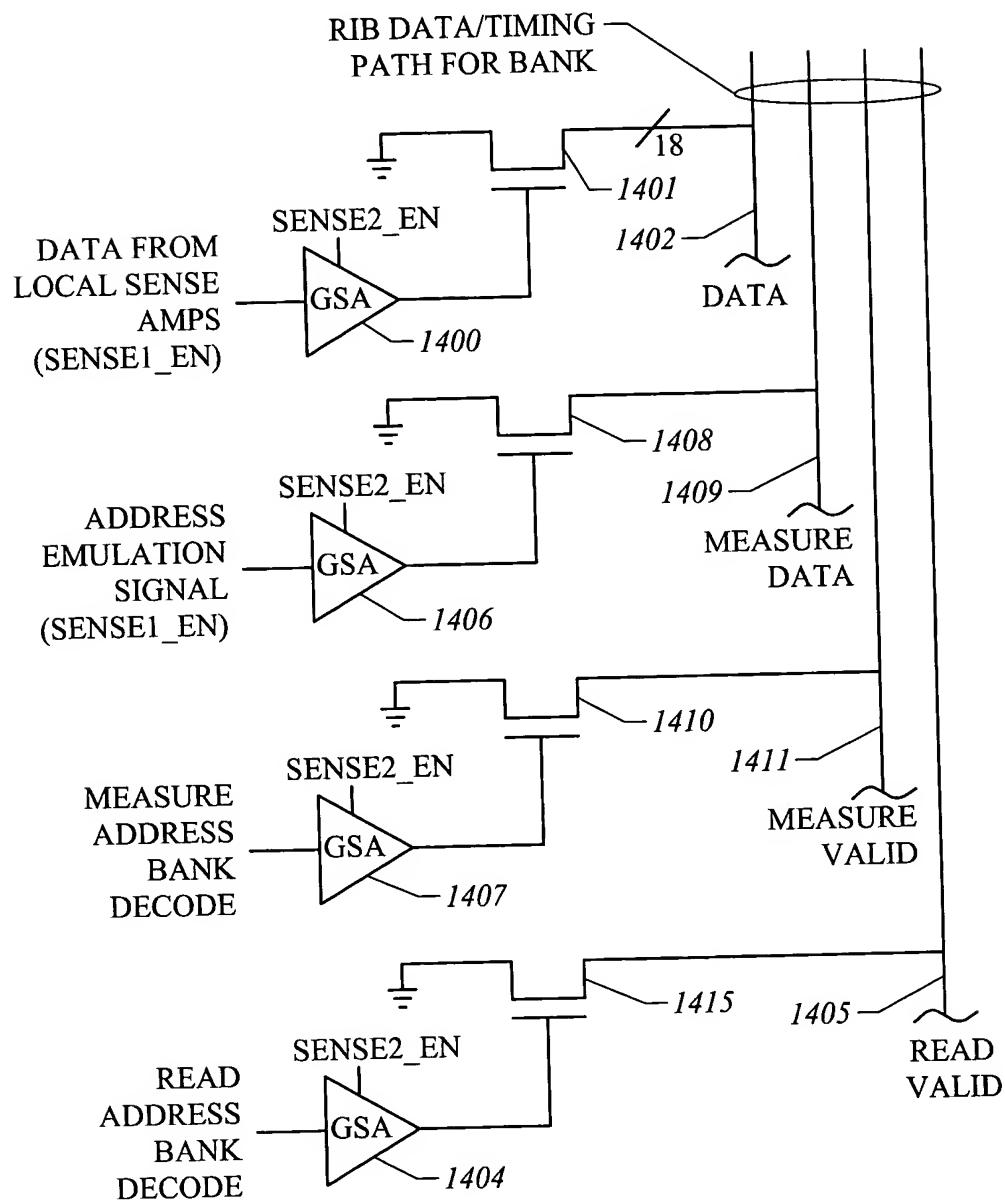


FIG. 14

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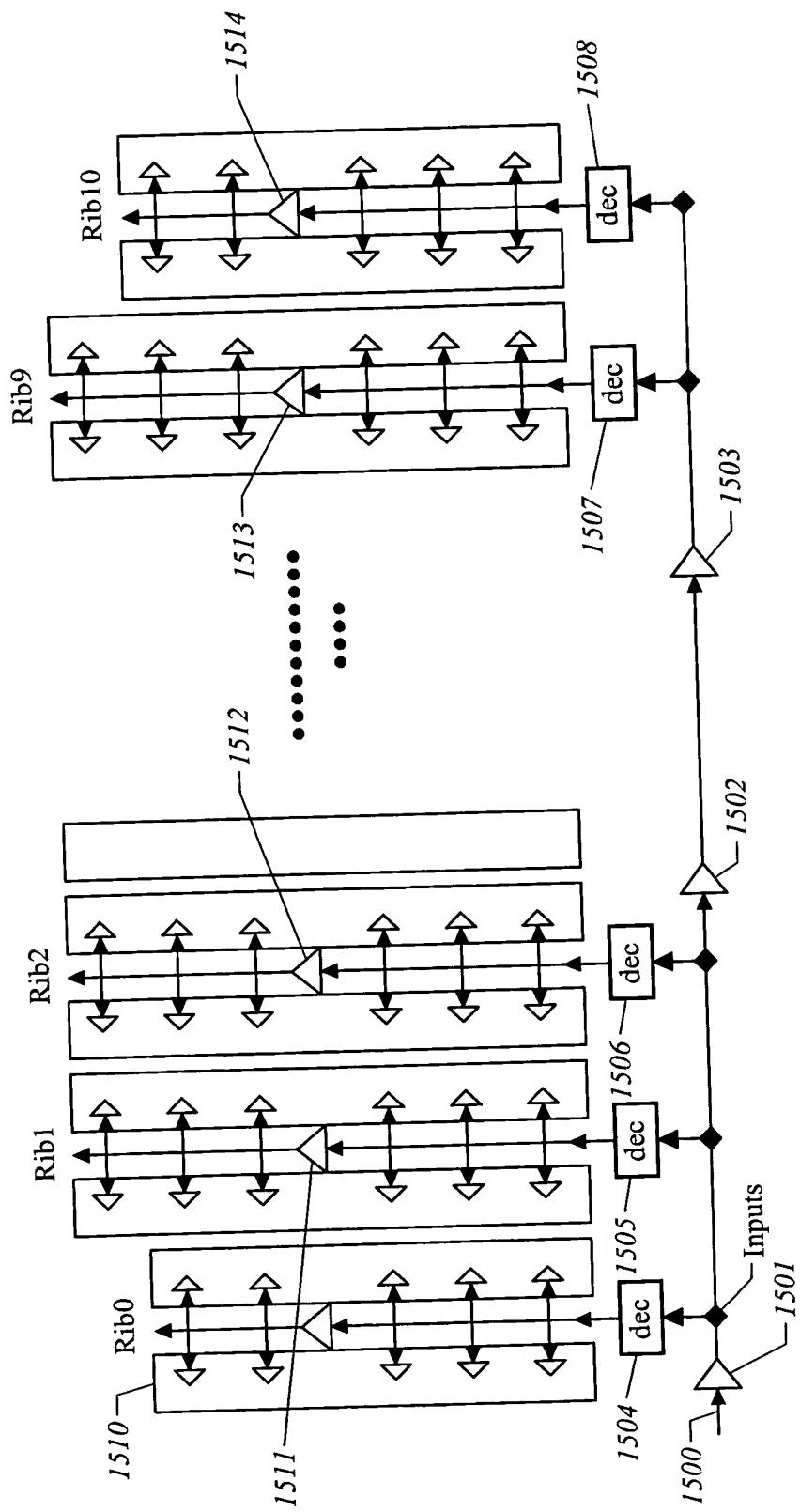
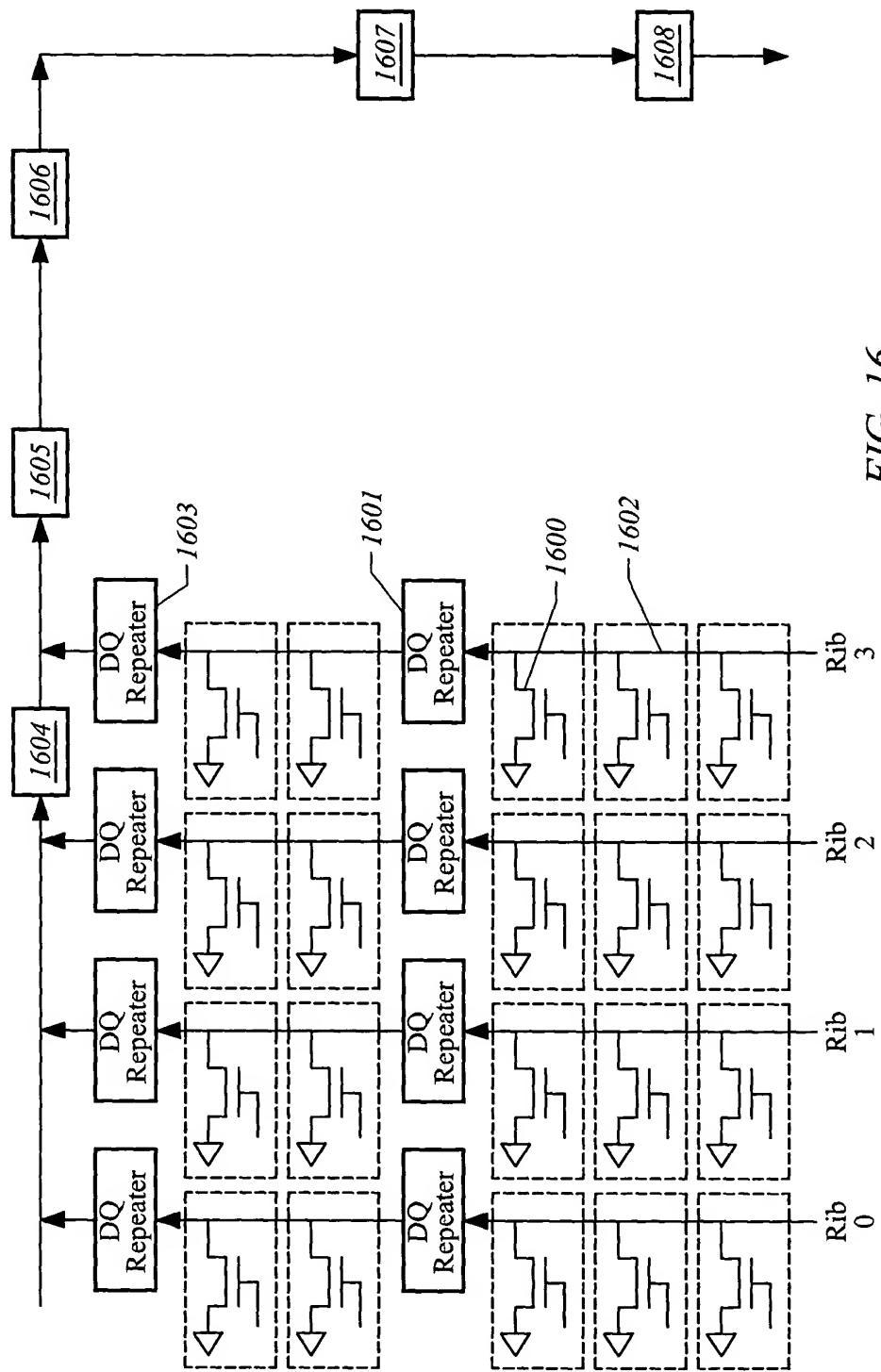


FIG. 15

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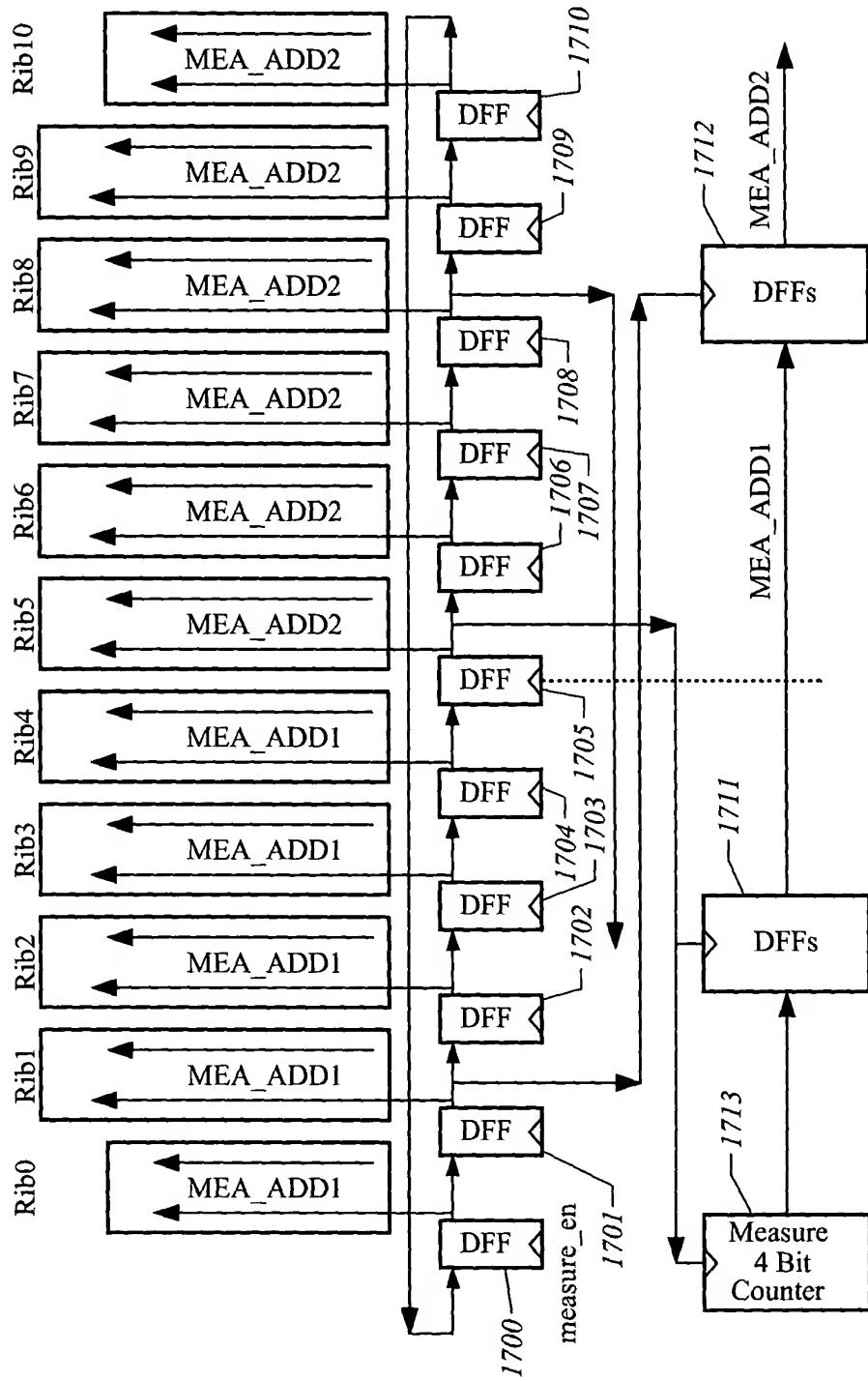


FIG. 17

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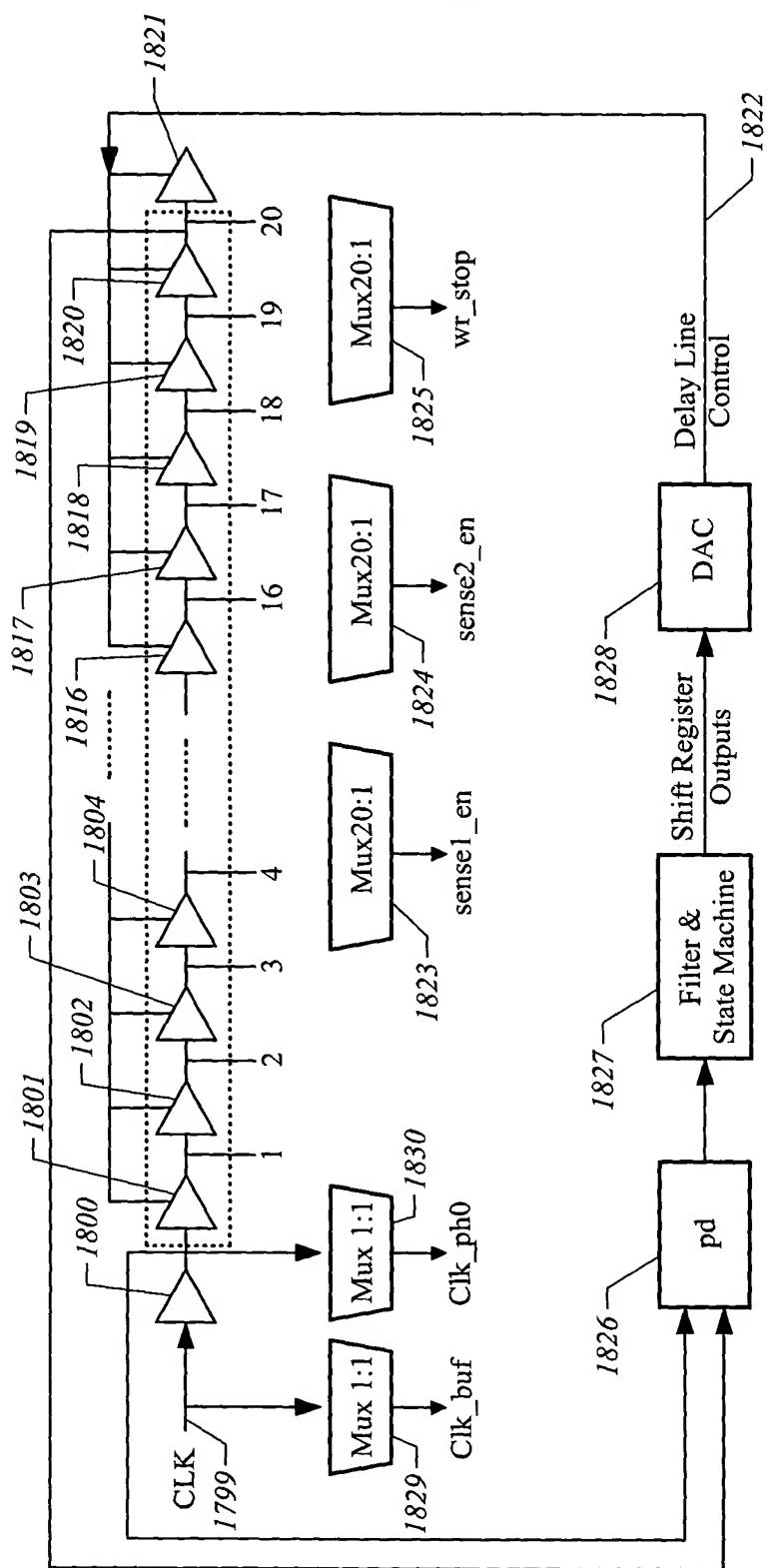


FIG. 18

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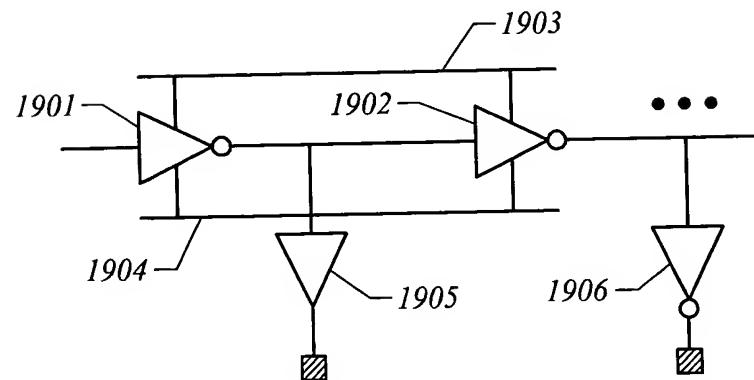


FIG. 19

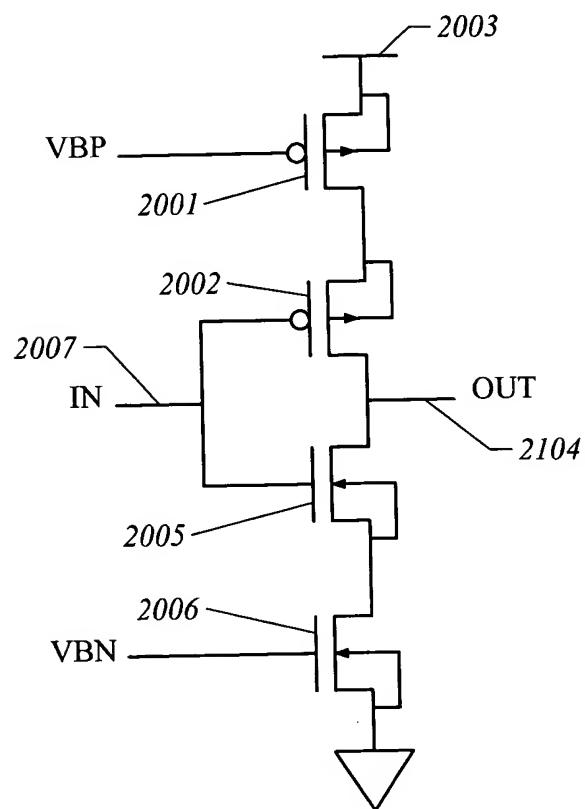


FIG. 20

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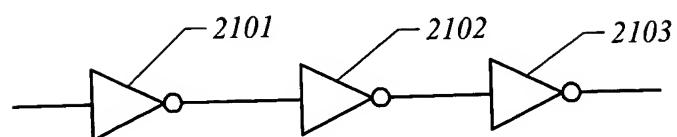


FIG. 21

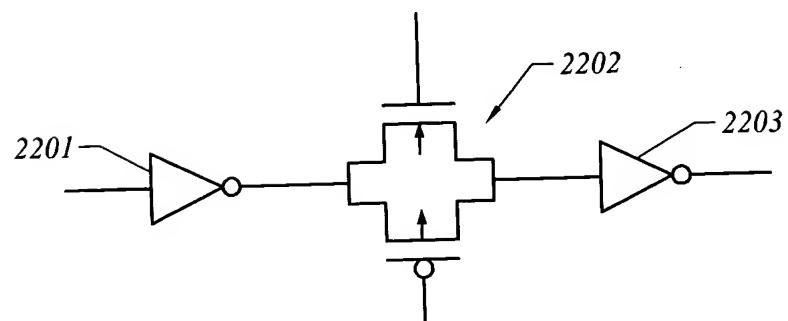


FIG. 22

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Lower Control Bits mux_s<4:0> mux_sp<4:0>					Higher Control Bits mux_sh<3:0> mux_shp<3:0>					cqf, aqf apf	
4	3	2	1	0	3	2	1	0			
X	X	X	X	X	0	0	0	0			
0	0	0	0	0	X	X	X	X			
0	0	0	0	1	0	0	0	1			In0
0	0	0	1	0	0	0	0	1			In1
0	0	1	0	0	0	0	0	1			In2
0	1	0	0	0	0	0	0	1			In3
1	0	0	0	0	0	0	0	1			In4
0	0	0	0	1	0	0	0	1			In5
0	0	0	1	0	0	0	0	1			In6
0	0	1	0	0	0	0	0	1			In7
0	1	0	0	0	0	0	0	1			In8
1	0	0	0	0	0	0	0	1			In9
0	0	0	0	1	0	1	0	0			In10
0	0	0	1	0	0	1	0	0			In11
0	0	1	0	0	0	1	0	0			In12
0	1	0	0	0	0	1	0	0			In13
1	0	0	0	0	0	0	1	0			In14
0	0	0	0	1	1	0	0	0			In15
0	0	0	1	0	1	0	0	0			In16
0	0	1	0	0	1	0	0	0			In17
0	1	0	0	0	1	0	0	0			In18
1	0	0	0	0	1	0	0	0			In19

FIG. 23

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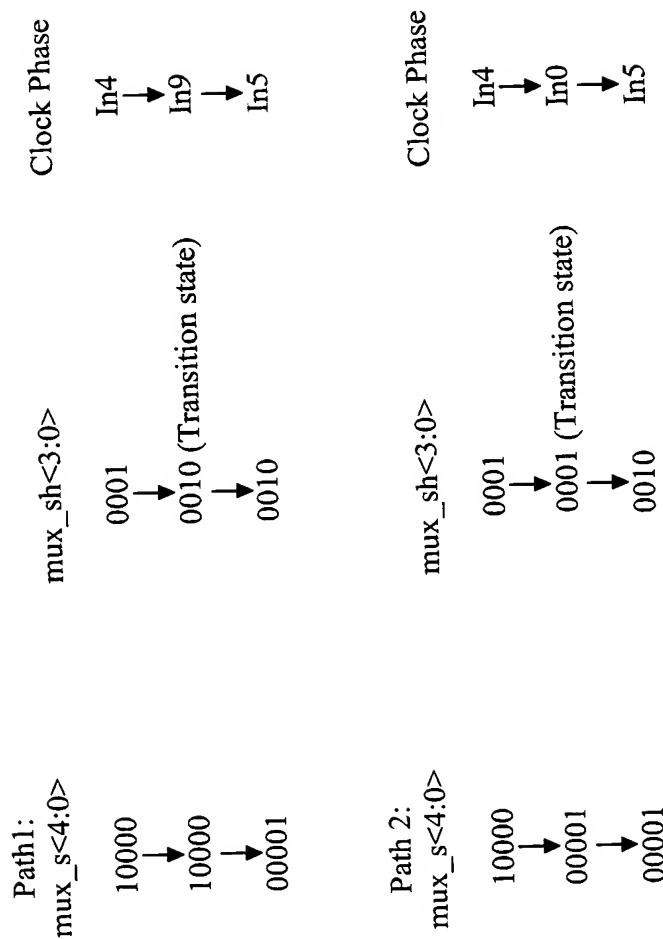


FIG. 24

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Lower Control Bits mux_s<4:0> mux_sp<4:0>					Higher Control Bits mux_sh<3:0> mux_shp<3:0>				cqd, aqf apf	
4	3	2	1	0	3	2	1	0	Clock phase	
X	X	X	X	X	0	0	0	0	Z	
0	0	0	0	0	X	X	X	X	Z	
0	0	0	0	1	0	0	0	1	In0	
0	0	0	1	0	0	0	0	1	In1	
0	0	1	0	0	0	0	0	1	In2	
0	1	0	0	0	0	0	0	1	In3	
1	0	0	0	0	0	0	0	1	In4	
1	0	0	0	0	0	0	0	1	In5	
0	1	0	0	0	0	0	1	0	In6	
0	0	1	0	0	0	0	1	0	In7	
0	0	0	1	0	0	0	1	0	In8	
0	0	0	0	1	0	0	1	0	In9	
0	0	0	0	1	0	1	0	0	In10	
0	0	0	1	0	0	1	0	0	In11	
0	0	1	0	0	0	1	0	0	In12	
0	1	0	0	0	0	1	0	0	In13	
1	0	0	0	0	0	0	1	0	In14	
1	0	0	0	0	1	0	0	0	In15	
0	1	0	0	0	1	0	0	0	In16	
0	0	1	0	0	1	0	0	0	In17	
0	0	0	1	0	1	0	0	0	In18	
0	0	0	0	1	1	0	0	0	In19	

FIG. 25

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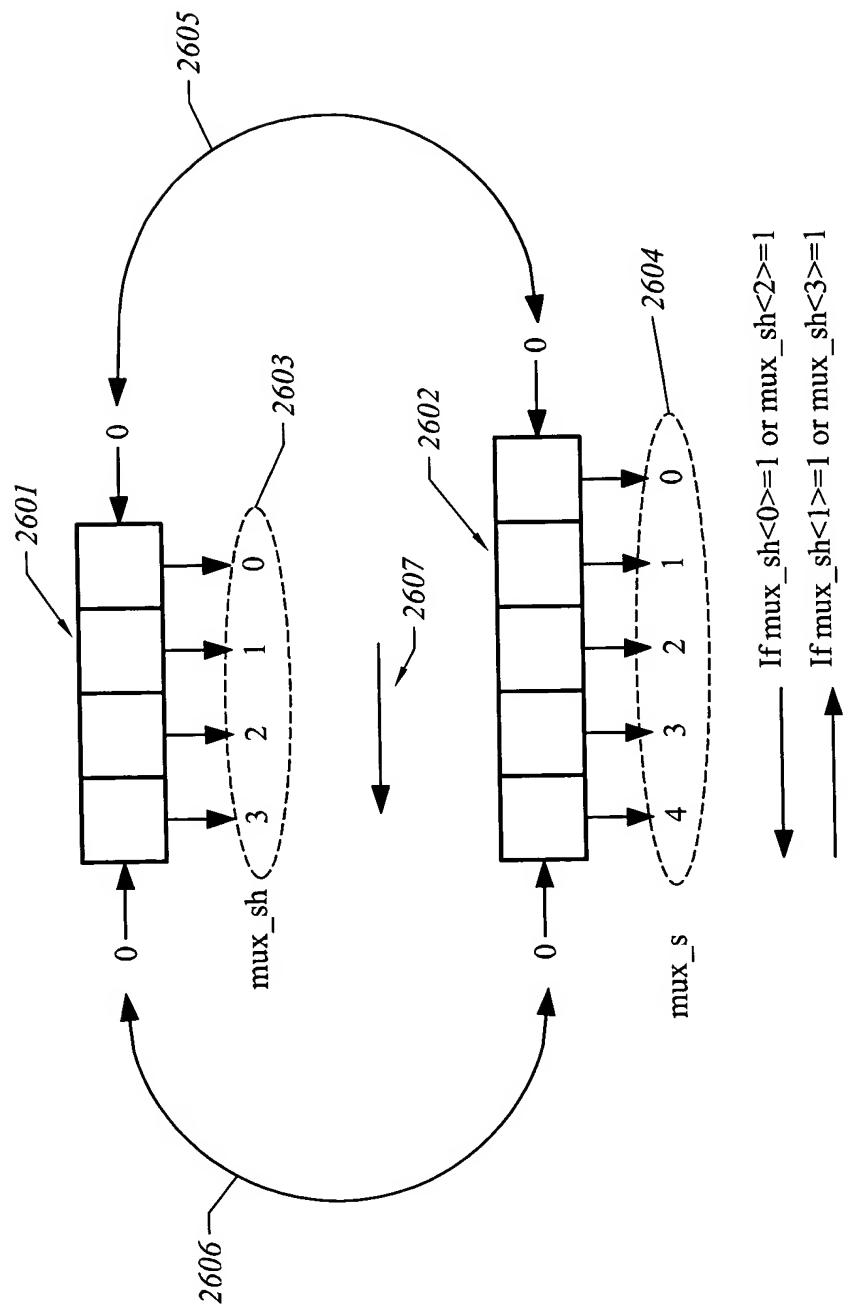


FIG. 26